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| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date : Thu Oct 17 09:48:09 2024

| Host : Samuel running 64-bit major release (build 9200)

| Command : report\_control\_sets -verbose -file hello\_world\_arty\_a7\_control\_sets\_placed.rpt

| Design : hello\_world\_arty\_a7

| Device : xc7a100ti

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Control Set Information

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1. Summary

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| Status | Count |

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| Number of unique control sets | 62 |

| Unused register locations in slices containing registers | 72 |

+----------------------------------------------------------+-------+

2. Histogram

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+--------+--------------+

| Fanout | Control Sets |

+--------+--------------+

| 1 | 1 |

| 4 | 3 |

| 5 | 2 |

| 6 | 1 |

| 8 | 3 |

| 9 | 2 |

| 13 | 1 |

| 14 | 1 |

| 16+ | 48 |

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3. Flip-Flop Distribution

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+--------------+-----------------------+------------------------+-----------------+--------------+

| Clock Enable | Synchronous Set/Reset | Asynchronous Set/Reset | Total Registers | Total Slices |

+--------------+-----------------------+------------------------+-----------------+--------------+

| No | No | No | 23 | 16 |

| No | No | Yes | 0 | 0 |

| No | Yes | No | 188 | 70 |

| Yes | No | No | 9 | 5 |

| Yes | No | Yes | 0 | 0 |

| Yes | Yes | No | 1548 | 565 |

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4. Detailed Control Set Information

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| Clock Signal | Enable Signal | Set/Reset Signal | Slice Load Count | Bel Load Count |

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| clock\_IBUF\_BUFG | | | 1 | 1 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/current\_state[3]\_i\_2\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 1 | 4 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_spi\_instance/curr\_state0 | 3 | 4 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_spi\_instance/bit\_count[3]\_i\_2\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_spi\_instance/cycle\_counter1 | 1 | 4 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_core\_instance/prev\_write\_request\_reg\_1[0] | 5 | 5 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_uart\_instance/reset\_internal | 3 | 5 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mcause[31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 6 | 6 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_spi\_instance/cycle\_counter[7]\_i\_1\_n\_0 | 2 | 8 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/mtimecmp[31]\_i\_2\_0[0] | reset\_debounced | 2 | 8 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/prev\_rw\_address\_reg[3]\_0[0] | reset\_debounced | 3 | 8 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_core\_instance/SR[0] | 3 | 9 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_uart\_instance/tx\_register | | 5 | 9 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_uart\_instance/tx\_register | 4 | 13 |

| clock\_50mhz\_BUFG | | reset\_debounced | 7 | 14 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mie\_mfie0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 7 | 19 |

| clock\_50mhz\_BUFG | | | 15 | 22 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mcause[31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mcause[30]\_i\_1\_n\_0 | 18 | 26 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mepc[31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 8 | 30 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_bus\_instance/E[0] | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 15 | 31 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mtvec1 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 18 | 31 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_uart\_instance/rx\_cycle\_counter[0]\_i\_1\_n\_0 | 8 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[15][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 13 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_minstret[31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 8 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mtval[31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 19 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[23][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 11 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_minstret[63]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 8 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/csr\_mscratch0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 19 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[3][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 9 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[21][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 14 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[11][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 12 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[17][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 12 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[10][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 9 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[12][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 8 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 10 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[14][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 12 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[16][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 12 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[1][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 8 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[22][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 11 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[27][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 13 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[28][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 12 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[13][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 11 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[25][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 9 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[29][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 10 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[2][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 11 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[26][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 12 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[18][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 14 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[30][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 13 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[24][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 8 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[9][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 10 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[6][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 10 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[5][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 14 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[7][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 9 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[4][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 12 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[8][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 10 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[20][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 10 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/mtimecmp[63]\_i\_2\_0[1] | reset\_debounced | 11 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/mtimecmp[63]\_i\_2\_0[0] | reset\_debounced | 7 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/prev\_rw\_address\_reg[1]\_0[0] | reset\_debounced | 13 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/integer\_file[19][31]\_i\_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 11 | 32 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_core\_instance/cr\_en\_reg[0] | reset\_debounced | 20 | 64 |

| clock\_50mhz\_BUFG | | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 35 | 98 |

| clock\_50mhz\_BUFG | rvsteel\_mcu\_instance/rvsteel\_bus\_instance/prev\_write\_request\_reg\_0[0] | rvsteel\_mcu\_instance/rvsteel\_core\_instance/reset\_internal\_1 | 41 | 101 |

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